REMARKS:

Claims 1-55 were presented for examination and were pending in this application. In an Official Action dated September 30, 2005, claims 1-55 were rejected. Applicants thank Examiner for examination of the claims pending in this application and addresses Examiner's comments below.

Applicants herein amend claims 1, 17, and 46. These changes are believed not to introduce new matter, and their entry is respectfully requested. The claims have been amended to expedite the prosecution of the application in a manner consistent with the Patent Office Business Goals, 65 Fed. Reg. 54603 (Sept. 8, 2000). In making these amendments, Applicants have not and do not narrow the scope of the protection to which Applicants consider the claimed invention to be entitled and do not concede that the subject matter of such claims was in fact disclosed or taught by the cited prior art. Rather, Applicants reserve the right to pursue such protection at a later point in time and merely seek to pursue protection for the subject matter presented in this submission.

Based on the above Amendment and the following Remarks, Applicants respectfully request that Examiner reconsider all outstanding objections and rejections, and withdraw them.

Response to Rejection Under 35 USC 102(e)

In the 3rd paragraph of the Office Action, Examiner rejects claims 1, 29-32, and 42-46 under 35 USC § 102(e) as allegedly being anticipated by U.S. Patent No. 6,542,991 to Joy et al. ("Joy"). This rejection is now traversed in view of the amended claims.

Based on the above Amendments and the following Remarks, Applicants respectfully submit that for at least these reasons claims 1, 29-32, and 42-46 are patentably

distinguishable over the cited reference. Therefore, Applicants respectfully request that Examiner reconsider the rejection, and withdraw it.

Claims 1, as amended, recites:

> a hardware thread scheduler for identifying which of said program threads said processor executes and configurable to allocate available processing time of the processor among at least the first and second program threads by causing thread-switching at a fixed time according to a predetermined fixed schedule, said schedule specifying that the first thread should be allocated processing time every first number of cycles and that the second thread should be allocated processing time every second number of cycles, wherein said first number of cycles is not equal to said second number of cycles.

The scheduler is configurable to cause the processor to switch from one thread to another thread at a fixed time according to a predetermined fixed schedule. This is greatly beneficial because it provides a predictable execution time for threads.

In contrast, Joy discloses "oblivious thread switching", in which the thread executed by the processor is switched every N cycles. (Col. 17, ln. 1-4) In the oblivious thread switching disclosed by Joy, a first thread would be executed every K cycles (where K is N times the number of threads in the oblivious switching rotation), a second thread would be executed every K cycles, and so on. The oblivious thread switching in Joy does not specify that a first thread should be allocated processing time every first number of cycles and the second thread should be allocated processing time every second number of cycles, wherein said first number of cycles is not equal to said second number of cycles, because in the oblivious thread switching of Joy every thread is executed every same number of cycles. Therefore, Joy fails to teach or disclose the predetermined fixed schedule as recited in claim 1.

Similary, Claim 46, as amended, recites:

switching the processor from the first thread state to the second thread state by coupling the execution pipeline from the first set of data storage devices to the second set of storage devices via the hardware thread selector at a fixed time according to a predetermined fixed execution schedule, said execution schedule specifying that the processor should switch to the first thread state every first number of cycles and that the processor should switch to the second thread state every second number of cycles, wherein said first number of cycles is not equal to said second number of cycles.

As discussed above, in the oblivious thread switching disclosed by Joy, the processor would switch to a first thread every K cycles, the processor would switch to a second thread every K cycles, and so on. The oblivious thread switching in Joy does not specify that the processor should switch to the first thread state every first number of cycles and that the processor should switch to the second thread state every second number of cycles, wherein said first number of cycles is not equal to said second number of cycles, because in the oblivious thread switching of Joy every thread is executed every same number of cycles. Therefore, Joy fails to teach or disclose the predetermined fixed execution schedule as recited in claim 46.

In a rejection under 35 U.S.C. §102, each and every claim element must be present in the applied reference. However, Examiner has failed to point out any prior "predetermined fixed schedule, said schedule specifying that the first thread should be allocated processing time every first number of cycles and that the second thread should be allocated processing time every second number of cycles, wherein said first number of cycles is not equal to said second number of cycles" and any prior "predetermined fixed execution schedule, said execution schedule specifying that the processor should switch to the first thread state every first number of cycles and that the processor should switch to the second thread state every

second number of cycles, wherein said first number of cycles is not equal to said second number of cycles." Therefore, it is respectfully submitted that the rejection of claims 1 and 46 is improper and should be withdrawn.

As claims 29-32 and 42-45 are dependent on claim 1, all arguments advanced above with respect to claim 1 are hereby incorporated so as to apply to claims 29-32 and 42-45.

Applicants respectfully submit that for at least these reasons claims 1, 29-32, and 42-46 are patentably distinguishable over the cited reference and request that the rejection be withdrawn.

Response to Rejection Under 35 USC 103(a) in View of Joy and Emer

In the 14th paragraph of the Office Action, Examiner rejects claims 2-3, 13-17, 19, and 21-24 under 35 USC § 103(a) as allegedly being unpatentable in view of Joy and U.S. Patent No. 6,493,741 to Emer et al. ("Emer"). This rejection is respectfully traversed.

Claim 17, as amended, recites:

> a hardware thread scheduler for identifying which of said program threads said processor executes and configurable to allocate available processing time of the pipelined processor among at least the first and second program threads according to an execution schedule;
> wherein said thread selection hardware in the pipelined processor switches from said first thread state to said second thread state between consecutive instruction cycles in response to the hardware thread scheduler identifying which of said program threads said processor executes.

Claim 19, similarly recites:

> switching the processor from executing the first program thread to executing the second program thread between the end of an execution cycles and before the beginning of a next consecutive execution cycle by coupling the execution pipeline from the first set of data storage devices to the second set of storage devices via the hardware thread selector.

Switching threads between consecutive instruction cycles beneficially allows switching between one program context and another without incurring any time penalty. Switching from one thread to another between the end of an execution cycles and before the beginning of a next consecutive instruction cycle beneficially allows switching to occur without the loss of any execution cycles.

It is important to note that switching threads "*between consecutive instruction cycles* in response to the hardware thread scheduler identifying which of said program threads said processor executes" does not specify how frequently thread switches occur, but rather how quickly the thread selection hardware executes those switches in response to the hardware thread scheduler. Thus, while the claim certainly includes the case of in which switching occurs every cycle, it should not be misunderstood as being limited to that particular case. Fundamentally, the question of *how long* a thread switch takes in response to a hardware thread scheduler should not be confused with the question *how often* a thread switch occurs. A disclosure of switching threads at every instruction cycle would not be sufficient to anticipate switching threads *between* consecutive instruction cycles.

As the Examiner correctly notes, Joy does not teach that "said selection hardware in the pipelined processor switches from said first thread state to said second thread state between consecutive instruction cycles in response to the hardware thread scheduler identifying which of said program threads said processor executes." Joy discloses "oblivious thread switching", in which the thread executed by the processor is switched every N cycles. (Col. 17, ln. 1-4) But this disclosure is an answer to the question of how often a thread switch occurs, and is not relevant to the claim element in question. The fact that a processor switches threads every N cycles has no bearing on the cost associated with those switches.

Joy teaches that "the thread switch logic supports a fast thread switch with a very small delay, for example three cycles or less." (Col. 16, ln. 61-62) Joy goes on to disclose an even more difficult constraint, "The thread switch logic generates the TID signal with a thread switch delay or overhead of one processor cycle." Thus, Joy discloses a very small delay in switching, but nonetheless Joy discloses a delay. Even the most ambitious portions of Joy teach the need of an overhead of at least one processor cycle. Therefore, Joy is fundamentally incompatible with switching without a time penalty, as Joy explicitly discloses that switching *between consecutive instruction cycles* in response to the hardware thread scheduler is not possible.

The deficiencies of Joy are not rectified by Emer. Emer discloses a multithreaded architecture in which thread switching occurs every cycle. As discussed above, the frequency of thread switching should not be confused with the overhead of thread switching. While Emer may disclose switching every execution cycle, Emer does not disclose switching between consecutive instruction cycles. In fact, Emer acknowledges that switching overhead has not been completely eliminated in the disclosed multithreaded architecture: "Multithreaded processors better tolerate long-latency operations, *effectively* eliminating vertical waste." (col. 1, ln. 58-60, emphasis added) As vertical waste has been only effectively eliminated, Emer suggests that in fact some number of cycles goes completely unused in the process of switching from one thread to another. (See Emer's definition of vertical waste, col. 1, ln. 41-42)

In considering what it means for vertical waste to be "effectively eliminated", it is important to consider the problem Emer sets out to solve. Emer describes multi-threaded

processor aimed to improve on the 15% of processor time estimated to be spent in spin loops, that is, waiting for a memory location to be updated. If processor stalls caused by long latency events can be reduced, significant improvements in the efficiency of the processor can result, and vertical waste will have been "effectively eliminated" despite that fact that some overhead will certainly exist while switching between one thread and another. Emer is concerned with using thread switches to reduce stalling, but Emer does not address the time the actual thread switches cost. Therefore, Emer does not teach or suggest "switching between consecutive instruction cycles."

Moreover, the combination of Joy and Emer does not disclose either the "thread selection hardware in the pipelined processor [switching] from said first thread state to said second thread state between consecutive instruction cycles" of claim 17 or the "switching...between the end of an execution cycle and before the beginning of a next consecutive instruction cycle" of claim 19. By combining the "at least one cycle" switch delay described in Joy, with the "effective" elimination of vertical waste of Emer, the teachings of the combined references amount to no more than what Joy discloses, that is, thread switching that requires an overhead of at least one cycle. Thus, the claimed thread switching "between consecutive instruction cycles" is not anticipated by the combined references. Therefore, Applicants submit that claims 17 and 19 are patentable over the cited art and request that the rejection be withdrawn.

As claims 2-3 and 13-16 are dependent on claim 17, all arguments advanced above with respect to claim 17 are hereby incorporated so as to apply to claims 2-3 and 13-16.

As claims 21-24 are dependent on claim 19, all arguments advanced above with respect to claim 19 are hereby incorporated so as to apply to claims 21-24.

Accordingly, for at least the reasons set forth above, claims 2-3, 13-17, 19, and 21-24 are patentable over the cited combined references. Thus, Applicants kindly request withdrawal of these rejections.

Response to Rejection Under 35 USC 103(a) in View of Joy, Emer, Borkenhagen, Ramakrishnan, and Gutgold

In the 27th, 29th, 36th, paragraphs of the Office Action, Examiner rejects claims 4-12, 18, 20, 25-28, under 35 USC § 103(a) as allegedly being unpatentable in view of Joy, Emer, and various combinations of U.S. Patent No. 6,567,839 to Borkenhagan et al. ("Borkenhagan"), U.S. Patent No. 6,085,215 to Ramakrishnan et al. ("Ramakrishnan"), U.S. Patent No. 6,026,503 to Gutgold et al. ("Gutgold").

Similary, in the 40th, 42nd, and 54th paragraphs of the Office Action, Examiner rejects claims 33-41, 47-55, under 35 USC § 103(a) as allegedly being unpatentable in view of Joy and various combinations of Borkenhagen, Ramakrishnan, and Gutgold. These rejections are respectfully traversed.

As claims 4-12 and 18 are dependent on claim 17, all arguments advanced above with respect to claim 17 are hereby incorporated so as to apply to claims 4-12 and 18. As claims 20, and 25-28 are dependent from claim 19, all arguments advanced above with respect to claim 19 are hereby incorporated so as to apply to claims 20, and 25-28.

Claim 17 and its dependent claims have been shown to be patentable over the combination of Joy and Emer, at least because the combination fails to disclose "a hardware thread... wherein said thread selection hardware in the pipelined processor switches from said first thread state to said second thread state between consecutive instruction cycles." Similarly, Claim 19 and its dependent claims have been shown to be patentable over the combination of Joy and Emer, at least because the combination fails to disclose "switching the processor from executing the first program thread to executing the second program thread between the end of an execution cycles and before the beginning of a next consecutive execution cycle." These deficiencies are not remedied by the various disclosures, either alone or in combination, of Borkenhagen, Ramkrishnan, and Gutgold.

As claims 33-41 are dependent on claim 1, all arguments advanced above with respect to claim 1 are hereby incorporated so as to apply to claims 33-41. As claims 47-55 are dependent from claim 46, all arguments advanced above with respect to claim 46 are hereby incorporated so as to apply to claims 47-55.

Claim 1 and its dependent claims have been shown to be patentable over Joy, at least because Joy fails to disclose "switching at a fixed time according to a predetermined fixed schedule, said schedule specifying that the first thread should be allocated processing time every first number of cycles and that the second thread should be allocated processing time every second number of cycles, wherein said first number of cycles is not equal to said second number of cycles." Similarly, Claim 46 and its dependent claims have been shown to be patentable over Joy, at least because Joy fails to disclose "switching the processor from the first thread state to the second thread state ... at a fixed time according to a predetermined fixed execution schedule, said execution schedule specifying that the processor should switch

to the first thread state every first number of cycles and that the processor should switch to the second thread state every second number of cycles, wherein said first number of cycles is not equal to said second number of cycles." These deficiencies are not remedied by the various disclosures, either alone or in combination, of Borkenhagen, Ramkrishnan, and Gutgold.

Examiner has cited Borkenhagen as allegedly teaching a processor switching between states by changing a state selection register. Borkenhagen discloses switching threads in response to a cache miss or external interrupt signal (Col. 6, ln. 22-42), said switches incurring the conventional "latency and performance penalties associated with switching threads." (Borkenhagen, col. 15, ln . 37-48). Borkenhagan does not disclose the deficiencies of Joy or the deficiencies of Joy in combination with Emer cited above.

Likewise, Ramakrishnan is cited to make up for Joy's lack of "thread identifier for identifying at least one hard-real-time (HRT) thread and at least one non-real-time thread" limitation. Ramakrishnan simply describes a software scheduler that uses a round robin approach to thread scheduling using conventional context switching. See Ramakrishnan, col. 9, ln. 9-10. The switching in Ramakrishnan, like in Borkenhagen, is conventional context switching that involves "an associated overhead in invoking the new thread." (Ramakrishnan, col. 12, lines 61-62, see also, col. 13, lines 6-7 "avoid time consuming context switching"). Ramakrishnan does not disclose the deficiencies of Joy or the deficiencies of Joy in combination with Emer cited above.

Finally, Gutgold is relied upon to provide the different access speed memory devices recited in claims 10-12 and 39-41 that are not explicitly described in Joy, Ramakrishnan, or

Emer. However, the combined reference still fails to teach or suggest the fixed time or consecutive-cycle context switching recited in the claims. Gutgold does not describe any context switching. Aside from the fact that Gutgold describes a microprocessor controlled system and associated microprocessor system components, Applicants see no other relation to Applicants' invention.

Accordingly, for at least the reasons set forth above, Applicants submit that claims 4-12, 18, 20, 25-28, 33-41, and 47-55 are patentable over the cited combined references and request that these rejections be withdrawn.

Conclusion

In sum, Applicants respectfully submit that claims 1 through 55, as presented herein, are patentably distinguishable over the cited references. Therefore, Applicants request reconsideration of the basis for the rejections to these claims and request allowance of them.

In addition, Applicants respectfully invite Examiner to contact Applicants' representative at the number provided below if Examiner believes it will help expedite furtherance of this application.

Respectfully Submitted,
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Date: Jan 30, 2006 By: _____

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